IN THE CLAIMS:

Please amend the claims as shown below.

Claims 1-21. (Cancelled)

22. (New) A computer system, comprising:

a primary chassis including a primary device disposed within the primary chassis, wherein the primary device includes a first bus coupled to a first electrical connector for conveying electrical signals;

a secondary chassis including a secondary device disposed within the secondary chassis, wherein the secondary device includes a second bus coupled to a second electrical connector for conveying the electrical signals;

wherein the first chassis and the second chassis are positioned substantially adjacent to one another; and

a bridge circuit board including a third connector and a fourth connector, wherein the bridge circuit board is positioned such that the third connector is detachably mated to the first connector and the second connector is detachably mated to the fourth connector, wherein the bridge circuit board further includes signal traces coupled to provide an electrical signal interconnection between the first bus and the second bus.

23. (New) The computer system as recited claim 22, wherein the first chassis and the second chassis are stacked one on top of the other.

24. (New) The computer system as recited claim 22, wherein the primary device is a motherboard.

25. (New) The computer system as recited claim 22, wherein the secondary device is

a device selected from the group consisting of a storage medium, a graphics processor, and a sound processor.

26. (New) The computer system as recited claim 22, wherein the bridge circuit board further includes a bridge circuit interposed between the third connector and the fourth connector and configured to provide an interface to the electrical signals conveyed between the first bus and the second bus.

27. (New) The computer system as recited claim 26, wherein the bridge circuit is further configured to receive the electrical signals conveyed on the first bus at a first bus speed and to transmit the electrical signals on the second bus at a second bus speed, and wherein the bridge circuit is further configured to receive the electrical signals conveyed on the second bus at a second bus speed and to transmit the electrical signals on the first bus at the first bus speed.

28. (New) The computer system as recited claim 26, wherein the bridge circuit is configured to translate the electrical signals conveyed using a first signal protocol to a second signal protocol.

29. (New) The computer system as recited claim 26, wherein the bridge circuit is a single integrated circuit chip.

30. (New) The computer system as recited claim 26, wherein the bridge circuit is implemented in a plurality of integrated circuit chips.

31. (New) The computer system as recited claim 22 further comprising a first power supply disposed within the primary chassis and a second power supply disposed within the secondary chassis, wherein the first power supply is configured to supply power to the primary device and the second power supply is configured to supply power to the secondary device.

32. (New) The computer system as recited claim 22 further comprising a first cooling device disposed within the primary chassis and a second cooling device disposed within the secondary chassis, wherein the first cooling device is configured to cool the primary device and the second cooling device is within the secondary device.

33. (New) A method for conveying electrical signals between a primary device and a secondary device, comprising:

conveying electrical signals on a first bus of a primary device disposed within a primary chassis, wherein the primary device includes a first electrical connector coupled to the first bus;

conveying electrical signals on a second bus of a secondary device disposed within a secondary chassis, wherein the secondary device includes a second electrical connector coupled to the second bus;

positioning the first chassis and the second chassis substantially adjacent to one another; and

providing an electrical signal interconnection between the first bus and the second bus using signal traces of a bridge circuit board including a third connector and a fourth connector, wherein the bridge circuit board is positioned such that the third connector is detachably mated to the first connector and the second connector is detachably mated to the fourth connector.

34. (New) The method as recited in claim 33, further comprising stacking the first chassis and the second chassis one on top of the other.

35. (New) The method as recited in claim 33, further comprising providing an interface to the electrical signals conveyed between the first bus and the second bus by interposing a bridge circuit between the third connector and the fourth connector on the bridge circuit board to.

36. (New) The method as recited claim 35, further comprising the bridge circuit receiving the electrical signals conveyed on the first bus at a first bus speed and transmitting the electrical signals on the second bus at a second bus speed, and the bridge circuit receiving the electrical signals conveyed on the second bus at a second bus speed and transmitting the electrical signals on the first bus at the first bus speed.

37. (New) The method as recited claim 35, further comprising translating the electrical signals conveyed using a first signal protocol to a second signal protocol using the bridge circuit.